ISO9001:2000 Certified SCI Quality System

Sierra Components, Inc.

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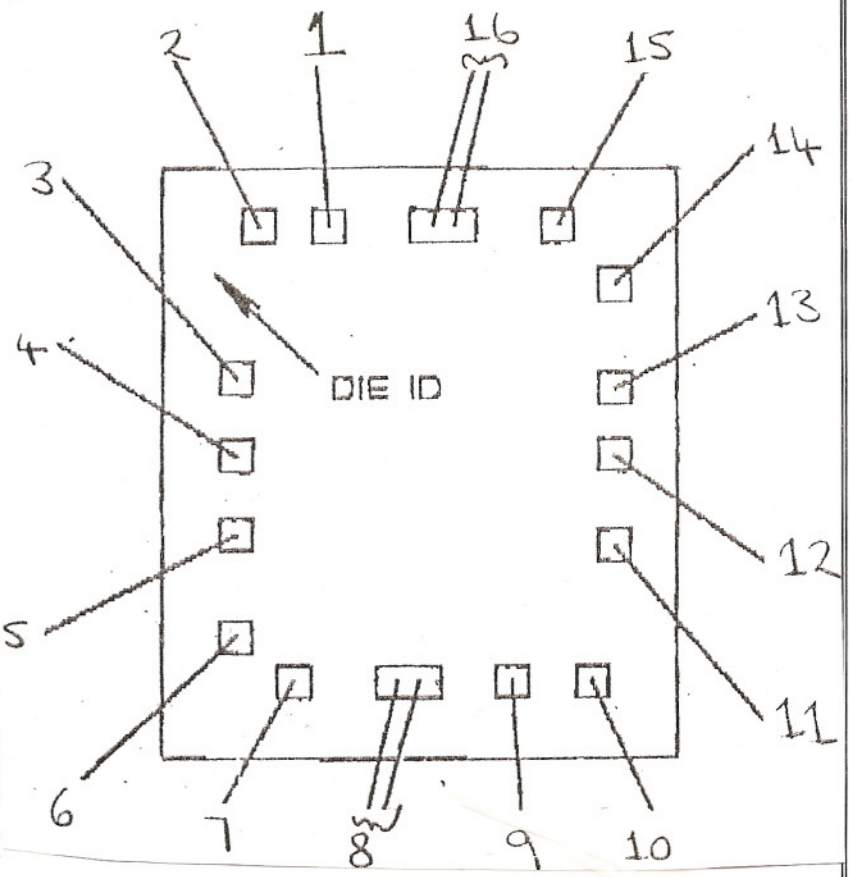
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

NOTE: CHIP BACK MUST BE CONNECTED TO GND.



Pad	Function	Pad	Function
1	INPUT A	9	INPUT C
2	OUTPUT A2	10	OUTPUT C2
3	OUTPUT A1	11	OUTPUT C1
4	ENABLE	12	ENABLE
5	OUTPUT B1	13	OUTPUT D1
6	OUTPUT B2	14	OUTPUT D2
7	INPUT B	15	INPUT D
8	GND	16	VCC

Topside Metal:
Backside:
Backside Potential:
Mask Ref:
Bond Pads (Mils):

APPROVED BY:	**DIE SIZE (Mils): 74 X 64 X 15**	**DATE: 3/20/00**
MFG: National	**THICKNESS:**	**P/N: DS26C31M**

DG 10.1.2
Rev A 3-4-99